8. (Currently Amended) The solid-state image sensing device described in Claim 7 wherein

said gate electrodes for read and said gate electrodes for reset of the facing light-receiving elements in the adjacent pixel rows are formed by a single electroconductive layer, and said electroconductive layer is arranged to zigzag between the adjacent pixel rows.

9. (Currently Amended) The solid-state image sensing device described in Claim 7 wherein

said first semiconductor regions of the light-receiving elements in the same pixel row are separated from each other by a fifth semiconductor region of the second electroconductive type that has an impurity concentration higher than said that of first semiconductor region.

10. (Currently Amended) The solid-state image sensing device described in Claim 9 further comprising

a plate electrode [[is]] formed via an insulating film on said fifth semiconductor region.

11. (Currently Amended) The solid-state image sensing device described in Claim 7 wherein

when a first voltage is applied to said gate electrode for reset, said light-receiving element is reset and the charge accumulated in said light-receiving element is evacuated, and when a second voltage is applied to said gate electrode for read, a signal corresponding to the charge accumulated in said light-receiving element is output.

12. (Currently Amended) The solid-state image sensing device described in Claim 7 wherein

said first, second and third semiconductor regions have p-type electroconductivity, while said semiconductor layer and said fourth semiconductor region have n-type electroconductivity.